Listing of claims:

Claims 1-20. (Canceled)

21. (Previously Presented) A method for conditioning a periodic analog signal to have positive and negative desired peak values, comprising:

detecting a peak value of the periodic analog signal; and

sequentially performing signal correction in a portion of a single period of the periodic analog signal to reduce a difference between the detected peak value and a desired peak value in a stepwise manner, the signal correction comprising:

multiplicative correcting by modifying the amplitude of the periodic analog signal; and

additive correcting by adding to the periodic analog signal a constant that changes the offset of the periodic analog signal in a positive or negative direction.

22. (Previously Presented) The method as claimed in Claim 21 wherein the signal correction comprises:

multiplicative correcting to amplify the periodic analog signal in a positive direction, and additive correcting to provide a signal offset to the periodic analog signal in a negative direction if the detected peak value is greater than the desired peak value within a positive part of a period of the periodic analog signal;

multiplicative correcting to amplify the periodic analog signal in a negative direction, and additive correcting to provide a signal offset to the periodic analog signal in a

positive direction if the detected peak value is less than the desired peak value within a positive part of a period of the periodic analog signal;

multiplicative correcting to amplify the periodic analog signal in a negative direction, and additive correcting to provide a signal offset to the periodic analog signal in a positive direction if the detected peak value is greater than the desired peak value within a negative part of a period of the periodic analog signal; and

multiplicative correcting to amplify the periodic analog signal in a positive direction, and additive correcting to provide a signal offset to the periodic analog signal in a negative direction if the detected peak value is less than the desired peak value within a negative part of a period of the periodic analog signal.

23. (Previously Presented) The method as claimed in Claim 21, wherein the sequence of signal correction is carried out at a frequency which is greater than the bandwidth of the periodic analog signal.

24. (Previously Presented) The method as claimed in Claim 21, further comprising temporarily storing the detected peak value of the periodic analog signal.

25. (Previously Presented) The method as claimed in Claim 21, further comprising:

detecting a zero crossing of a second periodic analog signal that is approximately 90 degrees out of phase relative to the periodic analog signal, the signal correction being performed following the detection of a zero crossing of the second periodic analog signal.

26. (Previously Presented) The method as claimed in Claim 25 wherein the periodic analog signal and the second periodic analog signal are sinusoidal signals such that the zero crossing of the second periodic analog signal substantially occurs when the periodic analog signal is at a peak value.

27. (Previously Presented) The method as claimed in Claim 21, wherein multiplicative correcting and additive correcting of signal correction occur at substantially the same time.

28. (Previously Presented) A method for conditioning a periodic analog signal to have positive and negative desired peak values, comprising:

detecting a peak value of the periodic analog signal;

selectively adjusting a reference signal in a stepwise manner from the desired peak value to approximately the detected peak value; and

sequentially performing signal correction in a portion of a period of the periodic analog signal to reduce a difference between the detected peak value and a desired peak value in a stepwise manner, the signal correction comprising:

multiplicative correcting by modifying the amplitude of the periodic analog signal; and

additive correcting by adding to the periodic analog signal a constant that changes the offset of the periodic analog signal in a positive or negative direction;

wherein a number of adjusting steps equals a number of signal correction steps, the periodic analog signal being modified in each signal correction step substantially the same as the reference signal is adjusted in each corresponding adjusting step.

29. (Previously Presented) The method of claim 28, wherein the sequence of signal correction is performed in a portion of a single period of the periodic analog signal.

30. (Previously Presented) A device, comprising:

a signal adjusting circuit that selectively amplifies a received first periodic analog signal and selectively generates a signal offset thereto; and

a comparison circuit that compares a peak value of the first periodic analog signal to an adjustable reference signal, and generates control signals based upon the comparison that control operation of the signal adjusting circuit to adjust received first periodic analog signal in each of a plurality of sequenced steps which occur within a portion of a single period of the periodic analog signal.

31. (Previously Presented) The device of claim 30, further comprising:

a peak value detector connected between the signal adjusting circuit and the comparison circuit that maintains a peak value of the output of the adjusting circuit until the peak value detector is reset.

32. (Previously Presented) The device of claim 30, wherein the comparison circuit comprises:

an adjustable reference source that generates the adjustable reference signal as an analog signal, the compare circuit adjusting the adjustable reference signal in sequential stepped levels between a predetermined value corresponding to a desired peak value and a peak value of the first periodic analog signal.

33. (Previously Presented) The device of claim 32, wherein the compare circuit comprises:

one or more storage elements that maintain one or more values corresponding to a number of stepped levels utilized in adjusting the reference signal.

34. (Previously Presented) The device of claim 33, wherein the signal adjusting circuit adjusts the amplitude and offset of the first periodic analog signal in a stepped manner based upon the values maintained in the one or more storage elements.

35. (Previously Presented) The device of claim 30, further comprising:

a second signal adjusting circuit to which a second periodic analog signal is supplied and which selectively amplifies the second periodic analog signal and selectively provides a signal offset thereto; and

a second comparison circuit coupled to an output of the second adjusting circuit for comparing a peak value of the second periodic analog signal to a second adjustable reference

signal, the compare circuit generating control signals that are based upon the comparison for controlling the second adjusting circuit so that the second periodic analog signal is adjusted by the second adjusting circuit in each of a plurality of steps, the plurality of steps occurring within a portion of the second periodic analog signal.

36. (Previously Presented) The device of claim 35, further comprising:

a zero detection circuit for receiving the first and second periodic analog signals, wherein the first and second periodic analog signals are approximately 90 degrees out of phase with each other, the signal adjusting circuit and the comparison circuit condition the first periodic analog signal upon the zero detection circuit detecting the second periodic analog signal crossing a zero reference, and the second signal adjusting circuit and the second comparison circuit condition the second periodic analog signal upon the zero detection circuit detecting the first periodic analog signal crossing the zero reference.

37. (Previously Presented) The device of claim 35, further comprising:

a third signal adjusting circuit to which a third periodic analog signal is supplied and which selectively amplifies the third periodic analog signal and selectively provides a signal offset thereto;

a third comparison circuit coupled to an output of the third adjusting circuit for comparing a peak value of the third periodic analog signal to a third adjustable reference signal, the compare circuit generating control signals that are based upon the comparison for controlling

the third adjusting circuit so that the third periodic analog signal is adjusted by the third adjusting circuit in a stepwise manner.

38. (Previously Presented) The device of claim 37, further comprising:

a level comparator circuit for comparing the first and second periodic analog signals and indicating when the first and second periodic analog signals are substantially the same, the third signal adjusting circuit and the third comparison circuit being initiated to adjust the third periodic analog signal by the level comparator.

39. (Previously Presented) The device of claim 35, further comprising:

phase correcting circuitry for adjusting a phase difference between the periodic analog signal and the second periodic analog signal, comprising circuitry for generating an auxiliary signal based upon the periodic analog signal and the second periodic analog signal and for incrementally displacing the phase between the periodic analog signal and the second periodic analog signal based upon the auxiliary signal.

40. (Previously Presented) A method, comprising:

performing a sequence of error detection operations on a reference signal in a stepwise manner during a portion of a period of a periodic analog signal so that the reference signal is adjusted from a predetermined level to a peak level of the periodic analog signal; and

performing a sequence of error correction operations on the periodic analog signal in a stepwise manner during a portion of a period of the periodic analog signal so that the

periodic analog signal is modified to be within a predetermined range of levels, each error correction operation comprising:

amplifying the periodic analog signal; and

offsetting to the periodic analog signal during the time the periodic analog signal is being amplified,

wherein an equal number of error correction and error detection operations are performed, and each error detection operation similarly adjusts the reference signal and the periodic analog signal.

41. (Previously Presented) The method of claim 40, wherein the error detection operations are performed on the reference signal prior to the error correction operations being performed on the periodic analog signal.

42. (Previously Presented) The method of claim 40, wherein the sequence of error detection operations are performed during a portion of a single period of the periodic analog signal.

43. (Previously Presented) A device, comprising:

an adjusting circuit that selectively amplifies a first periodic analog signal and selectively provides a signal offset thereto;

a compare circuit that compares a peak value of the first periodic analog signal to an adjustable reference signal and generates control signals based upon the comparison to

control the adjusting circuit so that the first periodic analog signal is adjusted in each of a plurality of steps which occur within a portion of a period of the periodic analog signal;

wherein the compare circuit comprises an adjustable reference source that generates the adjustable reference signal as an analog signal, the compare circuit adjusting the adjustable reference signal in sequential stepped levels between a predetermined value corresponding to a desired peak value and a peak value of the first periodic analog signal; and

one or more storage elements for maintaining one or more values corresponding to a number of stepped levels utilized in adjusting the reference signal.

44. (Previously Presented) A device, comprising:

a first adjusting circuit that selectively amplifies a first periodic analog signal and selectively provides a signal offset thereto;

a first compare circuit that compares a peak value of the first periodic analog signal to an adjustable reference signal and generates control signals based upon the comparison to control the adjusting circuit to adjust the first periodic analog signal in each of a plurality of steps which occur within a portion of a period of the periodic analog signal;

a second adjusting circuit that selectively amplifies a second periodic analog signal and selectively provides a signal offset thereto;

a second compare circuit that compares a peak value of the second periodic analog signal to a second adjustable reference signal and generates control signals based upon the comparison to control the second adjusting circuit to adjust the second periodic analog signal in each of a plurality of steps which occur within a portion of the second periodic analog signal;

a third adjusting circuit that selectively amplifies a third periodic analog signal and selectively provides a signal offset thereto;

a third compare circuit that compares a peak value of the third periodic analog signal to a third adjustable reference signal and generates control signals based upon the comparison to control the third adjusting circuit to adjust the third periodic analog signal in a stepwise manner; and

a level comparator circuit that compares the first and second periodic analog signals and indicates when the first and second periodic analog signals are substantially the same, the third adjusting circuit and the third compare circuit being initiated to adjust the third periodic analog signal by the level comparator.

45. (Previously Presented) A device, comprising:

a first adjusting circuit that selectively amplifies a first periodic analog signal and selectively provides a signal offset thereto;

a first compare circuit that compares a peak value of the first periodic analog signal to an adjustable reference signal and generates control signals based upon the comparison to control the adjusting circuit to adjust the first periodic analog signal in each of a plurality of steps occurring within a portion of a period of the periodic analog signal;

a second adjusting circuit that selectively amplifies a second periodic analog signal and selectively provides a signal offset thereto; and

a second compare circuit that compares a peak value of the second periodic analog signal to a second adjustable reference signal to generate control signals based upon the

comparison to control the second adjusting circuit to adjust the second periodic analog signal in each of a plurality of steps occurring within a portion of the second periodic analog signal; and

phase correcting circuitry that adjusts a phase difference between the first periodic analog signal and the second periodic analog signal by generating an auxiliary signal based upon the first periodic analog signal and the second periodic analog signal and incrementally displacing the phase between the first periodic analog signal and the second periodic analog signal based upon the auxiliary signal.

46. (Previously Presented) The device of claim 45, wherein the plurality of steps are performed during a portion of a single period of the periodic analog signal.